

FIG. 3

# NRZ DATA STREAM INPUTS

V1	<p>definite "1"</p> <p>"0" if both 2nd and 3rd bit value decisions are "1"</p> <p>"1" if only one of the 2nd and 3rd bit value decisions is a "1"</p> <p>"1" if both 2nd and 3rd bit values are "0"</p>
Vopt	<p>"1" if both 2nd and 3rd bit value decisions are "0"</p> <p>"0" if only one of the 2nd and 3rd bit value decisions is a "0"</p> <p>"0" if both 2nd and 3rd bit values are "1"</p>
V0	<p>definite "0"</p>

FIG. 4

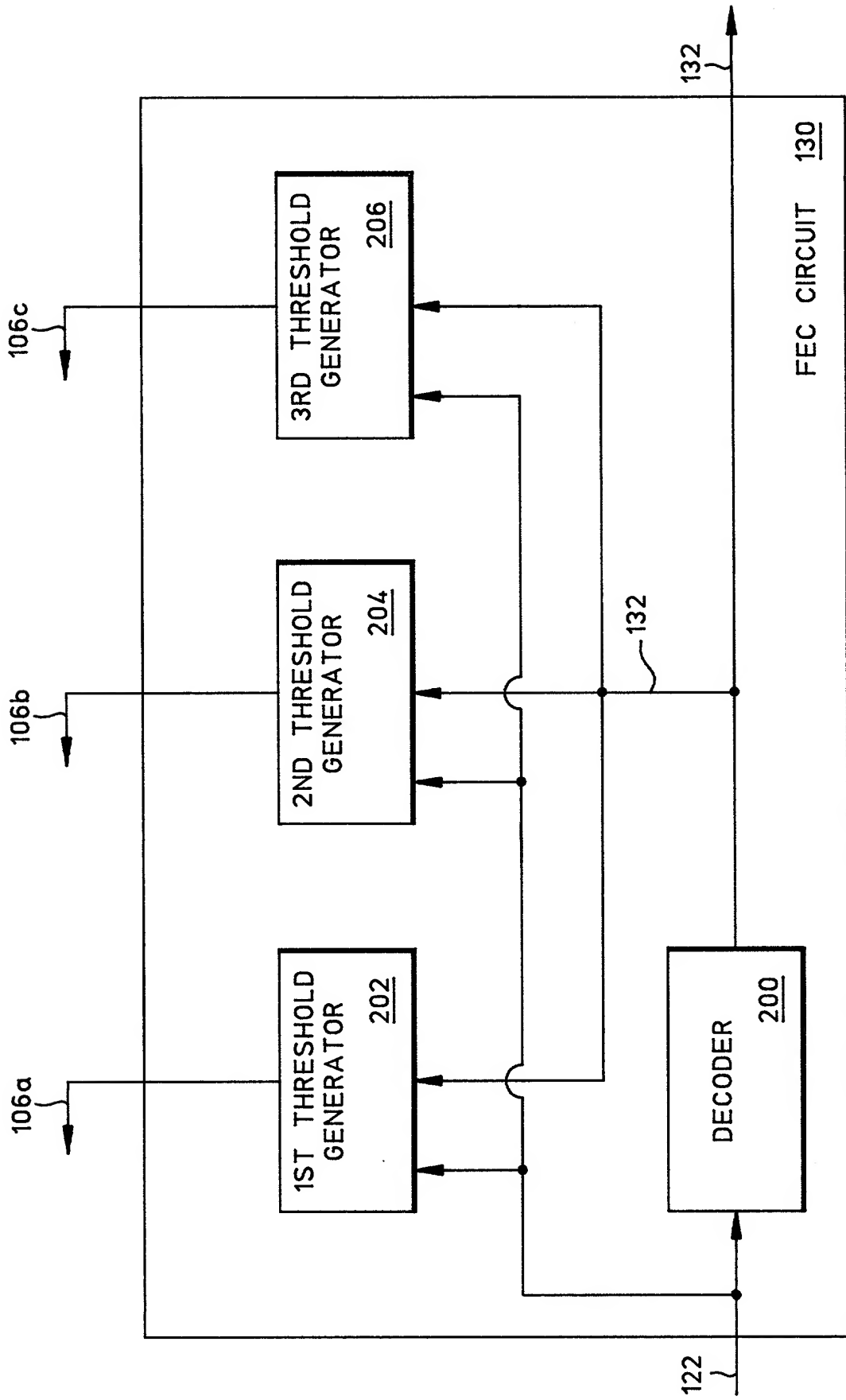


FIG. 5

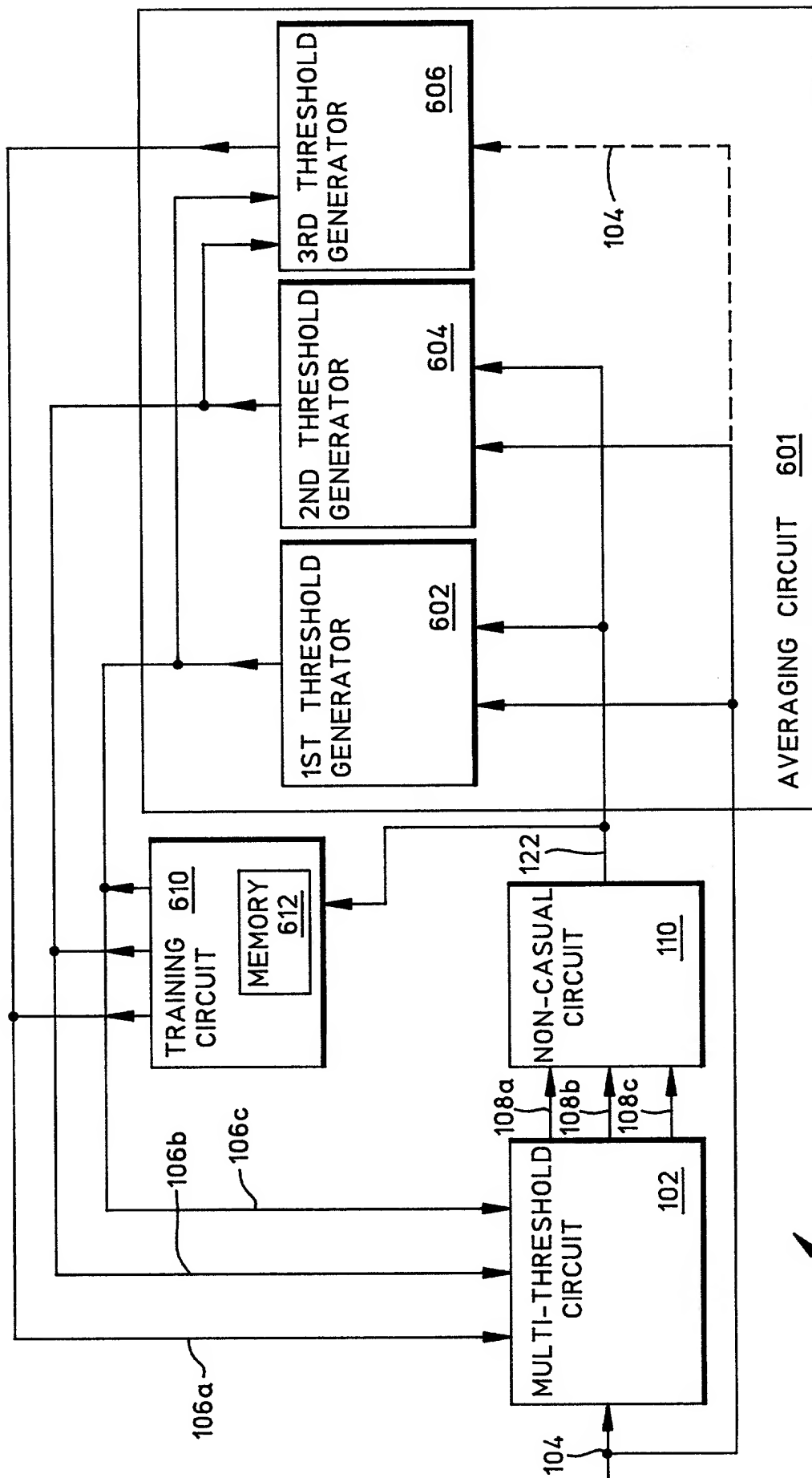


FIG. 6

110

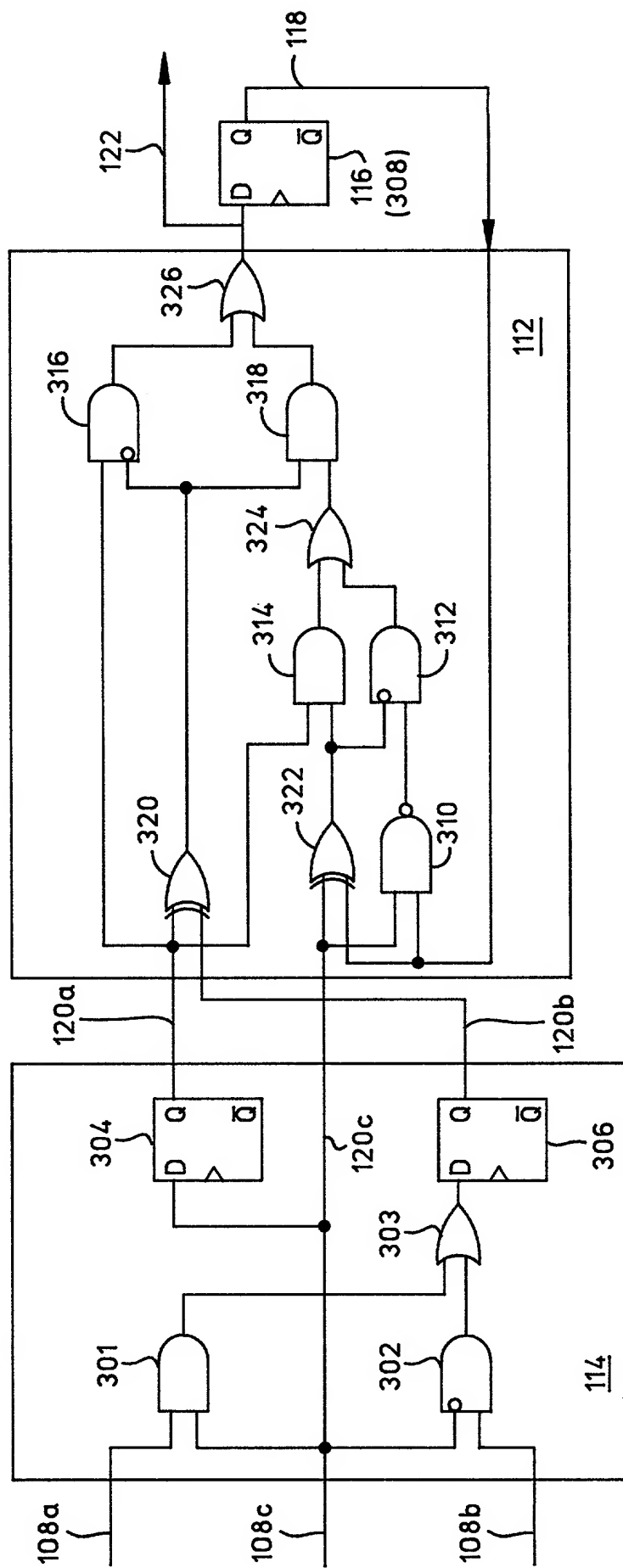


FIG. 7A

FIRST BIT ESTIMATE	Line 120a	120b	2ND BIT		3RD BIT		1ST BIT	
			Value		Value		Value	
	0	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	0
	0	0	1	1	0	0	0	0
	0	0	1	1	1	1	0	0
	0	1	0	0	0	0	1	0
	0	1	0	0	1	1	0	0
	0	1	1	1	0	0	0	0
	0	1	1	1	1	1	0	0
	1	0	0	0	0	0	1	1
	1	0	0	0	1	1	1	1
	1	0	1	1	0	0	1	1
	1	0	1	1	1	1	0	0
	1	1	0	0	0	0	1	1
	1	1	0	0	1	1	1	1
	1	1	1	1	0	0	1	1
	1	1	1	1	1	1	1	1

FIG. 7B

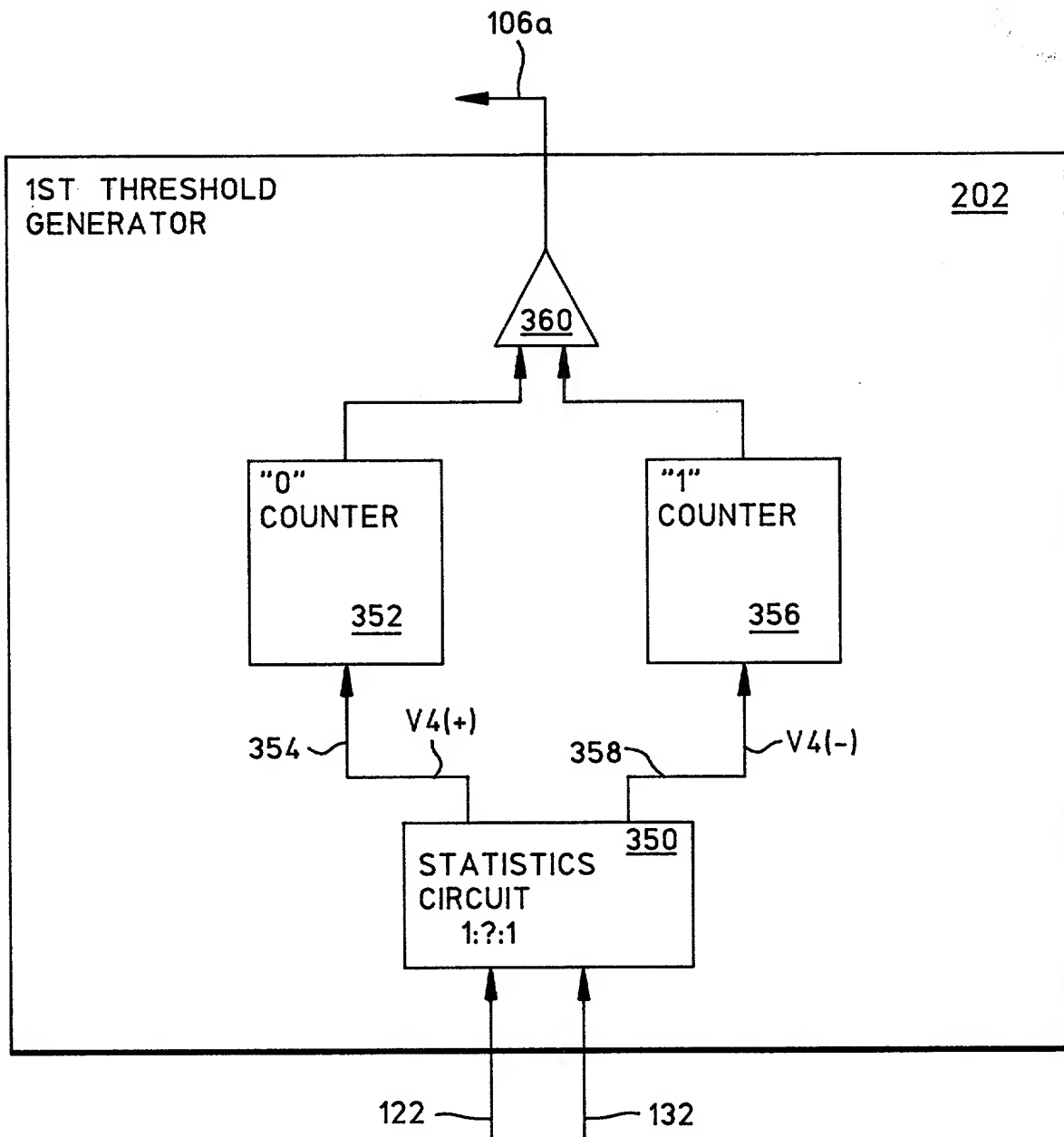
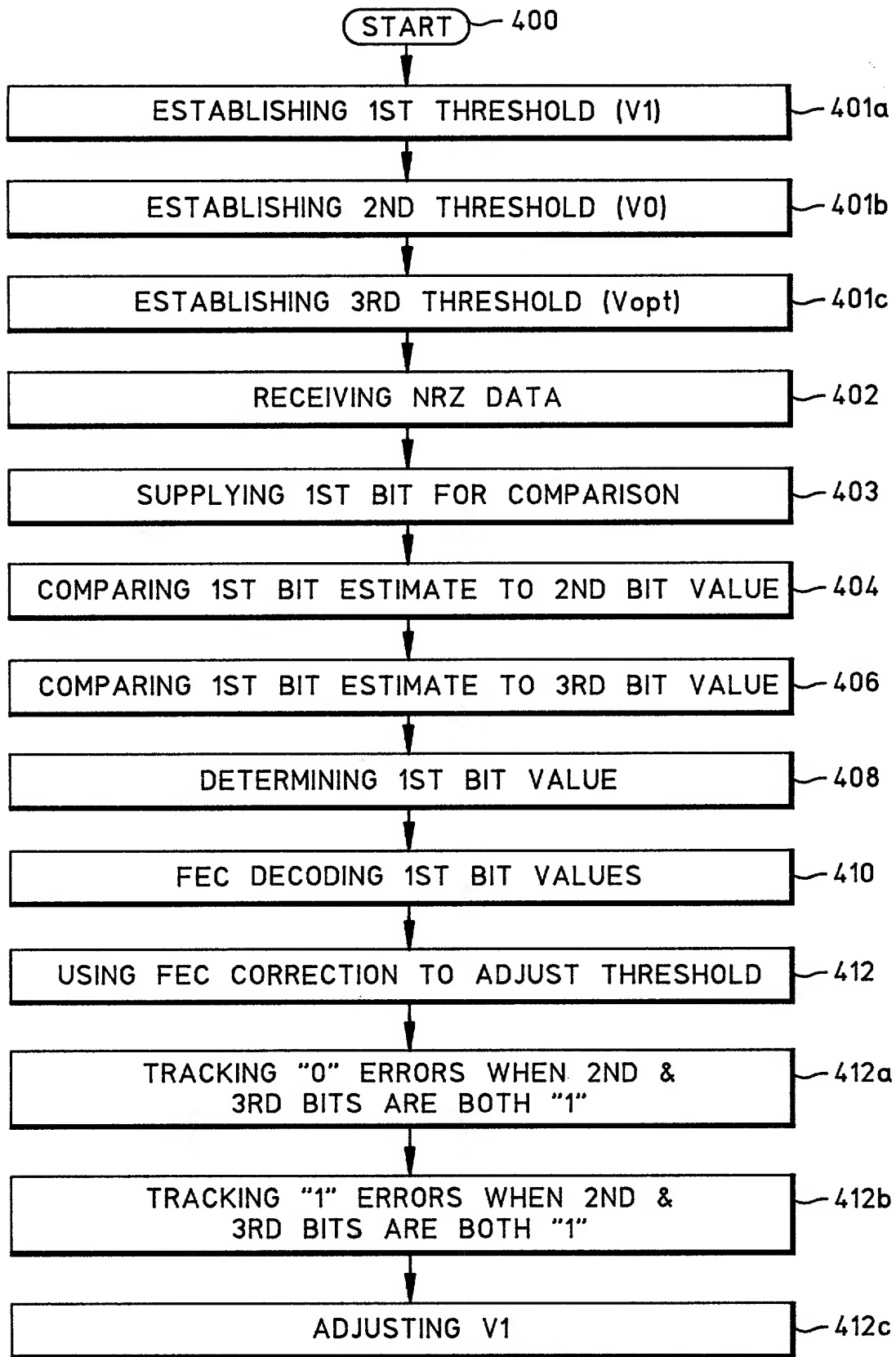


FIG. 8



Only One Correction per 3 bit sequence Error in the center bit					
Corrected Sequence	Graphic	Affected Counter		Action on Feedback	
		0 cntr	1 cntr	-	+
0 0 0		Cond 1 0 inc		V1 Toggle	
0 0 1		Cond 2 0 inc		V2 Toggle	
0 1 0			Cond 1 1 inc		V1 Toggle
0 1 1			Cond 2 1 inc		V2 Toggle
1 0 0		Cond 3 0 inc		V3 Toggle	
1 0 1		Cond 4 0 inc		V4 Toggle	
1 1 0			Cond 3 1 inc		V3 Toggle
1 1 1			Cond 4 1 inc		V4 Toggle

FIG. 9



TO FIG. 10B  
FIG. 10A

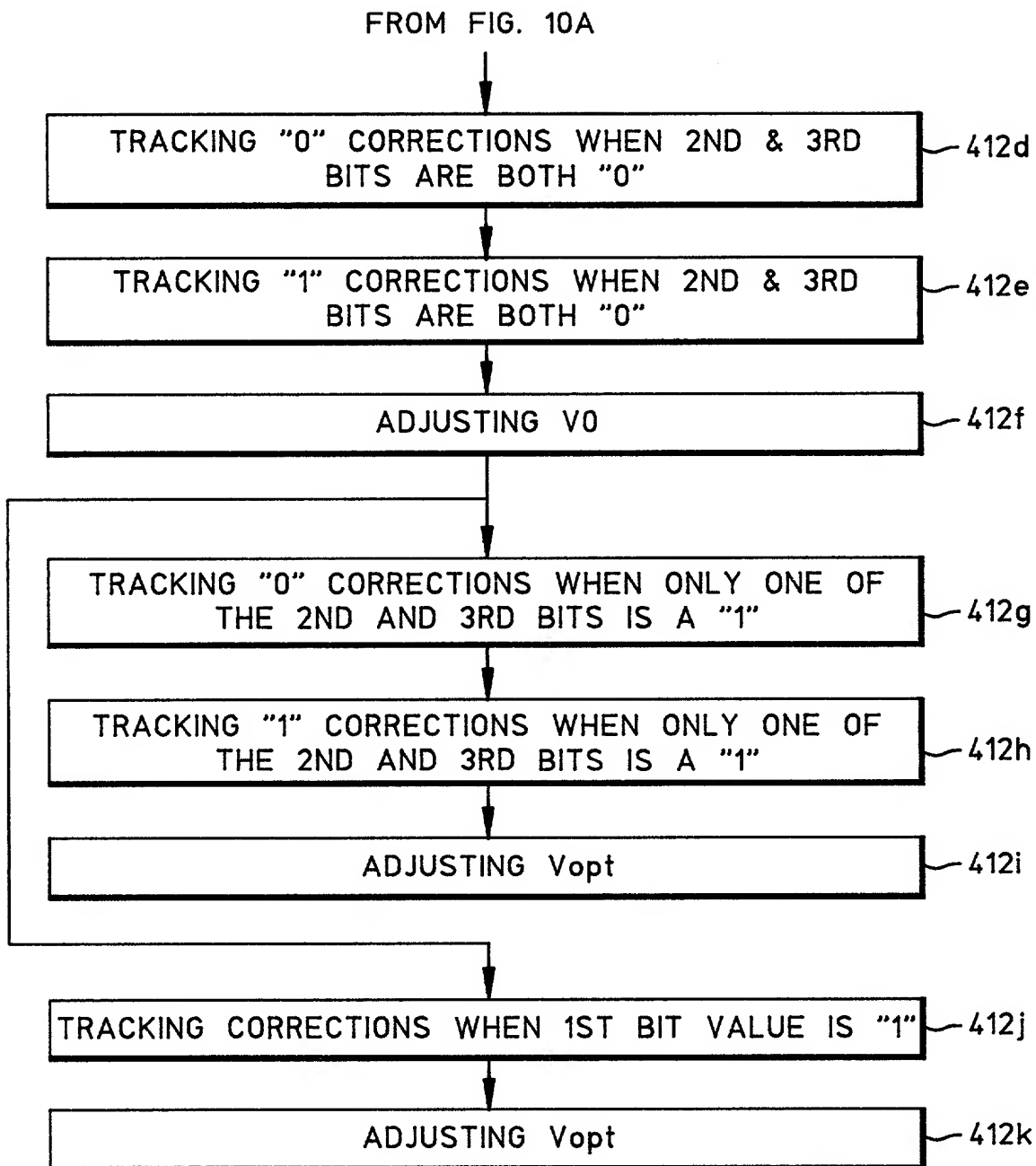


FIG. 10B

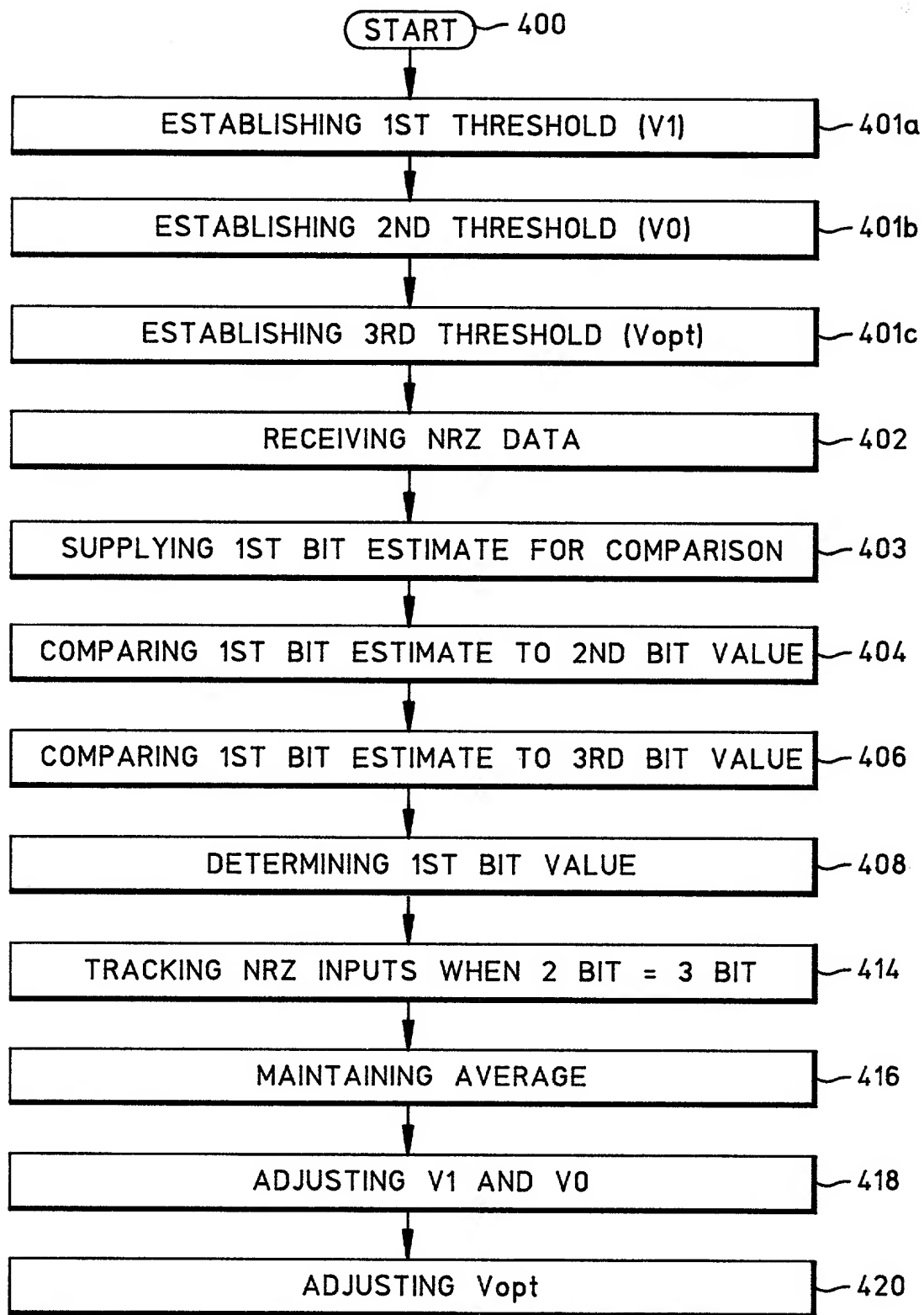


FIG. 11

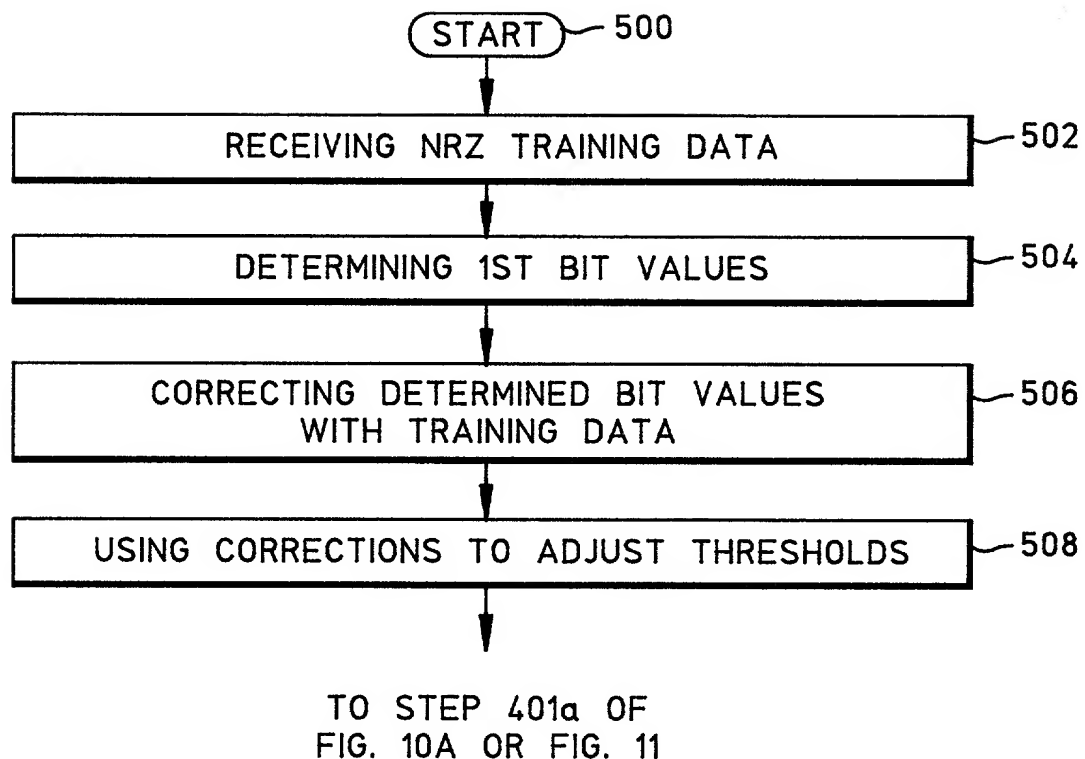


FIG. 12